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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/797,054	03/11/2004	Nobuo Karaki	119068	4701

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EXAMINER	
KARIMI, PEGEMAN	
ART UNIT	PAPER NUMBER
2629	
MAIL DATE	DELIVERY MODE
09/01/2009	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/797,054	KARAKI, NOBUO	
	Examiner	Art Unit	
	PEGEMAN KARIMI	2629	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *26 May 2009*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *23-36* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *23-36* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

1. The amendment filed on 05/26/2009 has been entered and considered by the examiner.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 23-30, 33, and 35 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yasukawa (U.S. Pub. No. 2001/0043175) in view of Dean (U.S. Patent No. 5,44,342).

As to claim 23, Yasukawa teaches a panel comprising:

a substratum (1, Fig. 1), ([0007], lines 1-3);

a plurality of scan lines (4) formed on the substratum (as can be seen in Fig. 1 the gate lines 4a are located on the substrate 1) ;

a plurality of data lines (7) intersecting with the plurality of scan lines ([0066], lines 3-4) wherein the plurality of data lines are formed on the substratum (as can be seen in Fig. 1 the data lines 7a are located on the substrate 1);

a plurality of pixels (pixels of the pixel region 20) disposed at locations where the plurality of scan lines intersect with the plurality of data lines (the pixels are defined in a

matrix pattern based on the location of the intersection of the gate and data lines, ([0086], lines 6-11); and

a peripheral circuit formed on the substratum ([0025]);

Yasukawa does not mention the peripheral circuit includes first and second processes. Dean teaches the peripheral circuit includes first and second processes (process of sending an output signal which, when active, indicates a transfer request to/from a connected coprocessor and an input signal, which indicates the completion of a coprocessor data transfer), and the first and second processes are controlled by means of event driving (col. 13, lines 57-63, the even is when the storage devices acknowledge receiving of its previous computation), and the first process requires the second process to forward data and the second process forwards the data to the first process (as can be seen in Fig. 46, the first process of sending request signal requires the second process to forward data signals "read data" and "acknowledge" and once the signals are forwarded the first process stops the "request" signal as indicated by number 7 in Fig. 46),

wherein the first process includes a first port, and the second process includes a second port (the first process has a first port for "CopReq_b" and "CopAck_b" and the second process has a second port "CopAck_b" and "CopReq_b", Fig. 45), and the first and second ports are connected via a channel (There is a channel connecting the first ports and second ports of "CopAck_b" and "CopReq_b" between the processor 400 and 504", and a req signal and an ack signal are sent or received between the first and second ports (col. 77, lines 50-53 and lines 60-65),

wherein the second port senses the req signal when the first port raises a level of the req signal from an L level to an H level (when the request signal is changed from an L level to an H level in step 2 of Fig. 46 the second port receives the request signal), and the second port raises a level of the ack signal from the L level to the H level when sensing the req signal (once the req signal is sensed the ack signal is raised from L level to an H level , which is step 4), and the first port senses a transition of the ack signal when the level of the ack signal is raised from the L level to the H level (in step 4 the first port senses the transition of signal ack and raised the ack signal from L level to H level), and the first port lowers the level of the req signal from the H level to the L level (once the signal ack is received then the first port of request port is changed from H level to the L level as can be seen in steps 5 and 6).

As to claim 24, Yasukawa teaches the peripheral circuit includes thin film transistors (the peripheral circuit such as a scanning side driving circuit and a data line driving circuit are formed on a substrate and include and connected to thin film transistors on the pixel region 20).

As to claim 25, Yasukawa teaches the panel comprising:

a scan line driver (22) for outputting scanning signals on the plurality of scan lines ([0086], lines 10-11) wherein the scan line driver is formed on the substratum (as can be seen in Fig. 5 the scan line driver is located on the substrate 1); and

a data line driver (21) for outputting data signals on the plurality of data lines ([0086], lines 8-10) wherein the data line driver is formed on the substratum (The data line driver is located on the substrate 1).

As to claim 26, Yasukawa teaches the substratum is a glass substratum ([0007], lines 1-3).

As to claim 27, Yasukawa teaches the peripheral circuit renders an image displayed by the plurality of pixels (the data line supplies image signal corresponding to image data to the data lines, which are connected to the pixels of the pixel region 20), ([0086], lines 6-11).

As to claim 28, Yasukawa teaches each of the plurality of pixels includes a switching element ([0012]).

As to claim 29, Dean teaches the peripheral circuit (500) includes a CPU (400).

As to claim 30, Dean teaches the peripheral circuit includes a memory (the peripheral circuit 500 includes memory 502).

As to claim 33, Yasukawa teaches the panel is a liquid crystal display panel ([0012]).

As to claim 35, an electronic device comprising the panel according to claim 23 (the cellular phone of Fig. 9(a) indicates an electronic device comprising the liquid crystal panel).

4. Claim 31 is rejected under 35 U.S.C. 103(a) as being unpatentable over Yasukawa in view of Dean, and further in view of Masteller (U.S. Patent No. 6,128,678).

As to claim 31, Masteller teaches the peripheral circuit includes a rendezvous circuit (761), and the first port includes an encoder (the first port of circuit 203 sends a signal as a code "Req out" to the circuit 228 in order for circuit 228 to decode the signal and sends out a decoded signal "ack out"), and the second port includes a decoder (second port refers to acknowledge signal being sent out by processor 228, wherein the input signal "REQUEST" is being decoded), and data is sent from the first port to the second port (the request data "REQ OUT" is sent from the first port to the second port), and the data received by the second port is input to the rendezvous circuit (once the "REQUEST signal is received by processor 228 the request signal is inputted into a rendezvous circuit 761 wherein the signals from 703, 708, and 707 are added via an AND gate 761). Therefore it would have been obvious to one of ordinary skilled in the art at the time the invention was made to have added the circuits 203 and 228 to the panel of Yasukawa as modified by dean because the rendezvous circuit in circuit 228 combines the signals of 708, 703, and 707, wherein the AND gate generates an acknowledge signal on signal line 704 if data is ready for transfer, and If no data is

ready in latches 752 and 754, a low signal from threshold gate 767 blocks the request until data is ready (col. 8, lines 56-60).

5. Claims 32, 34, and 36 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yasukawa in view of Dean, and further in view of Matsueda (U.S. Pub. No. 2003/0132896).

As to claim 32, Yasukawa and Dean do not mention the display device is an EL device. Matsueda teaches a display device comprising the panel according to claim 23, wherein the panel is an organic EL panel (the display device of Fig. 14 has gate lines, data lines, pixels and which are located on a glass substrate 16). Therefore it would have been obvious to one of ordinary skilled in the art at the time the invention was made to have added the structure of display device of Matsueda to the display device of Yasukawa as modified by dean because the active matrix substrate provided does not cause reduction in the brightness of electro-luminance elements and which comprises appropriate peripheral circuitry occupying a small area (abstract, lines 1-4).

As to claim 34, Matsueda teaches the panel is an electrophoretic panel (Matsueda teaches the active matrix is a method being used in panels such as electrophoretic elements), ([0004], lines 1-4).

As to claim 36, Matsueda teaches an electronic device comprising the display device (the portable telephone in Fig. 15A contains the display of EL device)

Response to Arguments

6. Applicant's arguments with respect to claims 23-36 have been considered but are moot in view of the new ground(s) of rejection.

The newly added references of Yasukawa (U.S. Pub. No. 2001/0043175), Dean (U.S. Patent No. 5,544,342), and Matsueda (U.S. Pub. No. 2003/0132896) have been added to read on the newly added claims 23-36.

Examiner would like to point out that the term "rendezvous circuit", the connection between the encoder and decoder should be explained in more details in claim 31 in order to overcome the prior art references.

Examiner would also like to point out to page 13 lines 5-6 of the specification, wherein by mentioning a limitation similar to "the Muller element performs a function so that a next transaction of sending and receiving request and acknowledge signals is not started until all the transactions that are in progress have ended" in claim 31 the applicant could overcome the prior art references.

Conclusion

7. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

8. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Horie (U.S. Pub. No. 2003/0095556) teaches The present invention has an object to perform transition signal control for creating asynchronous timing using the transition signal control circuit, which is comprised of Muller C elements with inverter.

Furber (U.S. Patent No. 5,918,042) teaches pipeline stage control circuit has an input request signal line, an input acknowledge signal line, an output request signal line and an output acknowledge signal line.

Inquiry

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to PEGEMAN KARIMI whose telephone number is (571)270-1712. The examiner can normally be reached on Monday-Thursday 9:00am - 5:30pm EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chanh Nguyen can be reached on (571) 272-7772. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Pegeman Karimi/
Examiner, Art Unit 2629
August 24, 2009

/Chanh Nguyen/
Supervisory Patent Examiner, Art Unit 2629